WHAT IS CLAIMED IS:

1. A method for forming a metal line of a semiconductor device comprising the steps of:

forming a via plug on a semiconductor substrate;

forming an interlayer insulating film on the semiconductor substrate, on which the via plug is formed;

forming a trench by patterning the interlayer insulating film in order to form an upper line to be connected to the via plug;

depositing a spacer insulating film, which is more invulnerable to a mechanical stress than the interlayer insulating film, on the semiconductor substrate on which the trench is formed;

forming a spacer on a side wall of the trench by performing an anisotropic-dry-etching of the spacer insulating film; and

forming a metal line by burying the trench with a conductive material.

2. The method of claim 1, wherein the spacer insulating film is formed by using an Si_3N_4 film or an SiC film which has a mechanical strength stronger than that of the interlayer insulation film and can be used as a metal diffusion barrier film.

3. The method of claim 2, wherein the spacer insulating film is deposited by using a plasma-enhanced chemical vapor deposition (PE-CVD) method at a temperature in the range of 200℃ to 450℃ under a pressure in the range of 0.01 torr to 500 torr.

4. The method of claim 1, wherein the spacer insulating film is deposited to have a thickness in the range of 50 Å to 1500 Å.

5. The method of claim 1, wherein the anisotropic-drying-etching is a reactive ion etching.

6. The method of claim 1, wherein the interlayer insulating film is an oxide film having a lower dielectric constant and formed by using an spin on glass (SOG) film, an fluorine doped tetra ethyl ortho silicate (F-TEOS) film, a carbon doped dielectric (COD) film or a porous low dielectric oxide film.

7. The method of claim 1, wherein the step of forming the via plug comprises the steps of:

forming a lower line on the semiconductor substrate;

forming a second interlayer insulating film on the semiconductor substrate, on which the lower line is formed;

forming a via hole by patterning the second interlayer insulating film in order to connect the lower line with the upper line; and

forming a via plug by burying the via hole with a conductive metal.

8. The method of claim 1, wherein the step of forming the metal line comprises the steps of:

depositing a diffusion barrier film along a step difference of the semiconductor substrate on which the spacer is formed;

depositing a copper seed layer on the diffusion barrier film;

forming a copper film on the copper seed layer by using an electroplating method, thereby burying an opening portion; and

forming the metal line by planarizing the copper film.